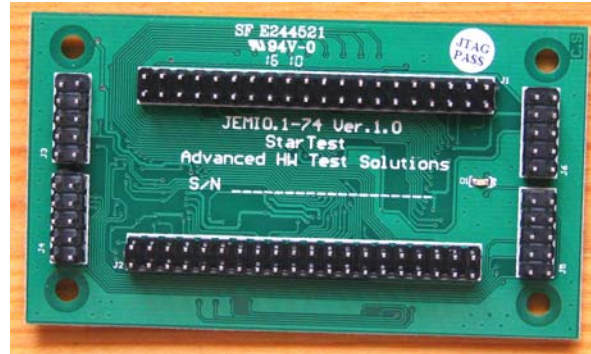


JEMIO

JTAG External Modules for Cluster Test



The **StarTest JEMIO** module main features are:

- ✓ Performs both Interconnect and Cluster tests in circuit boards
- ✓ Tests for opens all PWR and GND pins of the GPIO sets
- ✓ JTAG controlled GPIO nets for drive and sense
- ✓ Each I/O pin is independently controlled for sense, drive, bi-directional, and tri-state function
- ✓ Keyed flat connector compatibility
- ✓ Hot Swap: each module may be connected/disconnected between tests without switching power off
- ✓ Equipped with the JTAG/IEEE 1149.1 (**JEMIO.1**) and IEEE 1149.6 (**JEMIO.6**) Test Access Port (TAP)
- ✓ Supplied software contains BSDL file of the module
- ✓ Full compatibility with the following JTAG vendor ATPG and Runner platforms:

❖ Flynn Systems' **onTAP** Series 4000



❖ Corelis' **ScanExpress**



❖ JTAG Technologies' **ProVision**



❖ Asset' **ScanWorks**



❖ Goepel' **CASCON**



❖ XJTAG' **XJRunner**



EXPERIENCED TEST EXPERTS!

www.Start-Test.com



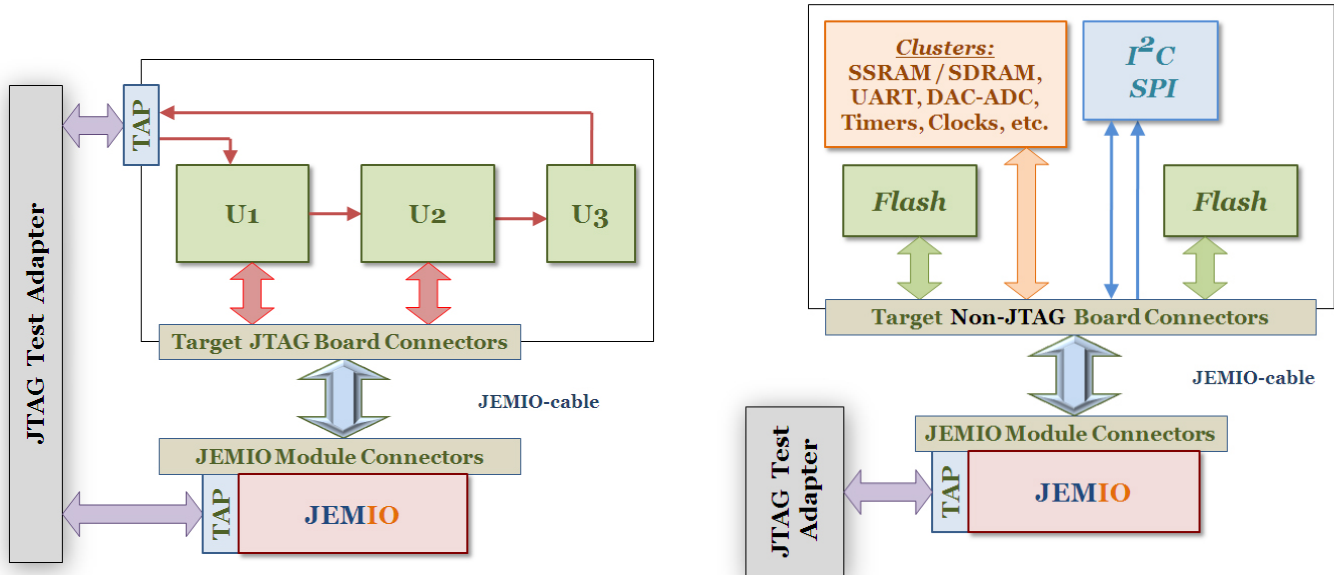
JEMIO

✓ Supports the wide range of GPIO net sets, including:

Module Name	Ordering Part Number
■ 74 pin JEMIO.1	JEMIO.1-74
■ 148 pin JEMIO.1	JEMIO.1-148
■ 34 pin JEMIO.1-LVDS	JEMIO.1-LVDS-34
■ yyy pin JEMIO.6	JEMIO.1-yyy
■ xx pin JEMIO.1-UD	JEMIO.1-UDxx

Consult [StarTest](#) for additional GPIO net sets (UDxx means — Upon Demand with xx IOs).

The **JEMIO** modules family provides a number of sets of JTAG accessible GPIOs or nets that can be used to control and observe signals that go off the board. Each JTAG channel is controlled individually and can be configured as an input, output, or tri-state. The **JEMIO** scan chain can be combined with the JTAG scan chains of the board being tested so it is included in the infrastructure verification and interconnect tests. Eventually, the **JEMIO** modules should be used separately or designed into the board or system test fixture. The **JEMIO** modules provide a flexible and low cost opportunity for JTAG test implementation for the board headers, edge connectors, PCB test points and pads, etc.



*JEMIO test setup
for JTAG boards*

*JEMIO test setup
for non-JTAG boards*