

4.20.16 - 144-Pin EP2-2100 DDR2 SDRAM 32b S0-DIMM Design Specification

EP2-2100 DDR2 SDRAM 32b-SO-DIMM

Reference Design Specification

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1. Product Description

This reference specification defines the electrical and mechanical requirements for the EP2-2100 memory module, a 144-pin, 267 MHz clock (533 MT/s data rate), 32-bit wide, Unbuffered Synchronous Double Data Rate 2 (DDR2) SDRAM 32-bit Dual In-Line Memory Module (DDR2 32b-SO-DIMM). It also defines a slower version, the EP2-1600, using 200 MHz clock (400 MT/s data rate) DDR2 SDRAMs. These DDR2 32b-SO-DIMMs are intended for use in cost sensitive, low pin count applications such as peripheral devices.

Reference design examples are included which provide an initial basis for 32b-SO-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 267MHz clock rate support. Other designs are acceptable, and all 32b-SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Product Family Attributes

Attribute:	Values:	Notes:
32b-SO-DIMM Organization	x 32	
32b-SO-DIMM Dimensions (nominal)	30.0 mm high, 67.60 mm wide / MO-274 variation AA	
32b-SO-DIMM Types Supported	Unbuffered	
Pin Count	144	
Pin pitch	0.8 mm	
DDR SDRAMs Supported	256 Mb, 512 Mb, 1 Gb	
Capacity	64 MB, 128 MB, 256 MB, 512 MB, 1 GB	
Serial Presence Detect	Should be consistent with JEDEC latest Revision	
Voltage Options, Nominal	1.8 V V_{DD} 1.8 V V_{DDQ} 1.8 V to 3.3 V V_{DDSPD}	1
Interface	SSTL_18	
Note 1: V_{DDSPD} is not tied to V_{DD} or V_{DDQ} on the DDR2 32b-SO-DIMM.		

Raw Card Summary

Raw Card	Number of DDR SDRAMs	SDRAM Organization	Number of Ranks
A	2 or 4	x16	1 or 2
B	4 or 8	x8	1 or 2

2. Environmental Requirements

PC2-2100 DDR2 SDRAM Unbuffered 32b-SO-DIMMs are intended for use in computing peripheral environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK[1:0]	Clock Inputs, positive line	2	DQ[31:0]	Data Input/Output	32
$\overline{\text{CK}}$ [1:0]	Clock inputs, negative line	2	DM[3:0]	Data Masks	4
CKE[1:0]	Clock Enables	2	DQS[3:0]	Data strobes	4
$\overline{\text{RAS}}$	Row Address Strobe	1	$\overline{\text{DQS}}$ [3:0]	Data strobes	4
$\overline{\text{CAS}}$	Column Address Strobe	1	TEST	Logic Analyzer specific test pin (No connect on 32b-SO-DIMM)	1
$\overline{\text{WE}}$	Write Enable	1			
$\overline{\text{S}}$ [3:0]	Chip Selects	4	V _{DD}	SDRAM Core and I/O Power	13
A[9:0],A[11:15]	Address Inputs	15	V _{SS}	Common Ground	30
A10/AP	Address Input/Autoprecharge	1	V _{REF}	Input/Output Reference	1
BA[2:0]	SDRAM Bank Address	3	V _{DD} SPD	SPD Power	1
ODT[3:0]	On-die termination	4	NC,V _{REFCA}	V _{REFCA} for future use	1
SCL	Serial Presence Detect (SPD) Clock Input	1			
SDA	SPD Data Input/Output	1	NC	Reserved for future use	12
SA[2:0]	SPD address	3			Total: 144

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/ $\overline{\text{CK0}}$, CK1/ $\overline{\text{CK1}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S}}[3:0]$	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 by $\overline{\text{S1}}$; Rank 2 by $\overline{\text{S2}}$; Rank 3 by $\overline{\text{S3}}$.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR2 SDRAM internal bank of four or eight is activated.
A[9:0], A10/AP, A[15:11]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
ODT[3:0]	Input	Active high	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ if enabled via the DDR2 SDRAM mode register.
DQ[31:0]	In/Out	—	Data Input/Output pins.
DM[3:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
$\overline{\text{DQS}}[3:0]$, DQS[3:0]	In/Out	All edges	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. When the DDR2 SDRAM is programmed via mode register for differential data strobe, timing is relative to the crosspoint of associated DQS and $\overline{\text{DQS}}$ signals.
VREF	Supply	—	Supply reference voltage for SSTL_18 inputs.
V _{DD} , V _{DDSPD} , V _{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and common ground for the module.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V _{DDSPD} on the system planar to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM.
SA[2:0]	Input	—	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (32b-SO-DIMMs).

DDR2 SDRAM 32b-SO-DIMM Pinout

Pin#	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REF}	2	NC, V _{REFCA}	49	DQ3	50	CK0#	99	DQ13	100	V _{SS}
3	V _{SS}	4	NC	51	V _{SS}	52	V _{SS}	101	V _{SS}	102	CK1
5	DQ16	6	NC	53	NC, DQS0#	54	NC, CKE1	103	DQ14	104	CK1#
7	DQ17	8	NC	55	DQS0	56	V _{DD}	105	DQ15	106	V _{SS}
9	V _{SS}	10	NC	57	V _{SS}	58	NC, ODT0	107	V _{SS}	108	NC, S1#
11	DQ18	12	NC	59	DM0	60	CKE0	109	DQ24	110	V _{DD}
13	DQ19	14	NC	61	V _{SS}	62	WE#	111	DQ25	112	BA0
15	V _{SS}	16	NC	63	DQ4	64	V _{DD}	113	V _{SS}	114	A1
17	DQS2#	18	NC	65	DQ5	66	NC, S3#	115	DQ26	116	A5
19	DQS2	20	NC	67	V _{SS}	68	BA1	117	DQ27	118	V _{DD}
21	V _{SS}	22	V _{DD}	69	DQ6	70	A10/AP	119	V _{SS}	120	A9
23	DM2	24	NC, A14	71	DQ7	72	V _{DD}	121	DQS3#	122	A12
25	V _{SS}	26	NC, A13	73	V _{SS}	74	A3	123	DQS3	124	V _{DD}
27	DQ20	28	A11	75	DQ8	76	A7	125	V _{SS}	126	NC
29	DQ21	30	V _{DD}	77	DQ9	78	NC, A15	127	DM3	128	NC
31	V _{SS}	32	A6	79	V _{SS}	80	V _{DD}	129	V _{SS}	130	NC
33	DQ22	34	A2	81	DQ10	82	RESET#	131	DQ28	132	V _{SS}
35	DQ23	36	CAS#	83	DQ11	84	A8	133	DQ29	134	SDA
37	V _{SS}	38	V _{DD}	85	V _{SS}	86	A4	135	V _{SS}	136	SA0
KEY				87	NC, DQS1#	88	V _{DD}	137	DQ30	138	SA1
39	V _{SS}	40	NC, S2#	89	DQS1	90	A0	139	DQ31	140	SA2
41	DQ0	42	V _{DD}	91	V _{SS}	92	NC, BA2	141	V _{SS}	142	SCL
43	DQ1	44	NC, ODT1	93	DM1	94	S0#	143	NC, TEST	144	V _{DD} SPD
45	V _{SS}	46	V _{SS}	95	V _{SS}	96	V _{DD}				
47	DQ2	48	CK0	97	DQ12	98	RAS#				

Note: NC = No Connect.

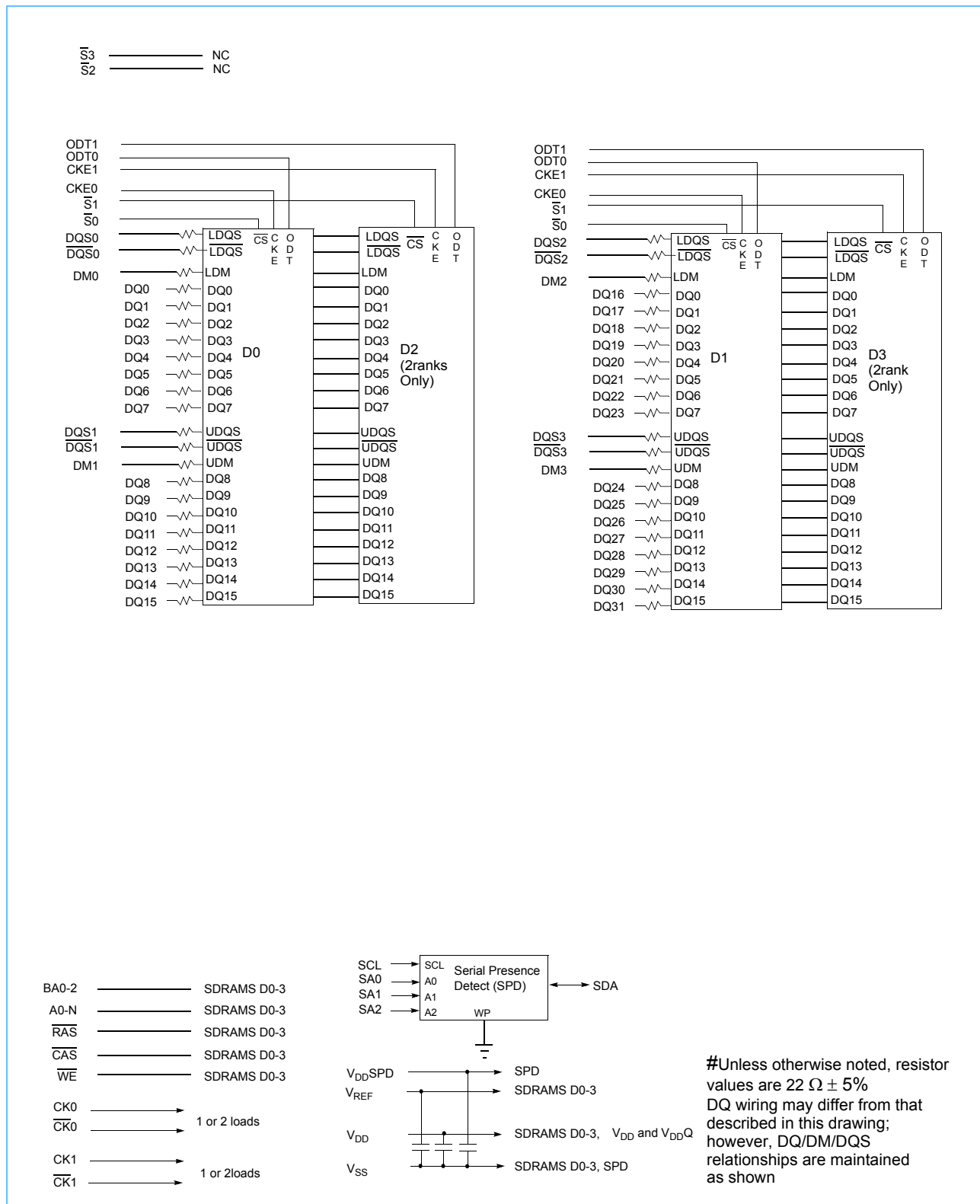
Note: NC,TEST(pin 143) is for bus analysis tool and is not connected on normal memory modules.

Note: RESET# not used on modules without PLL.

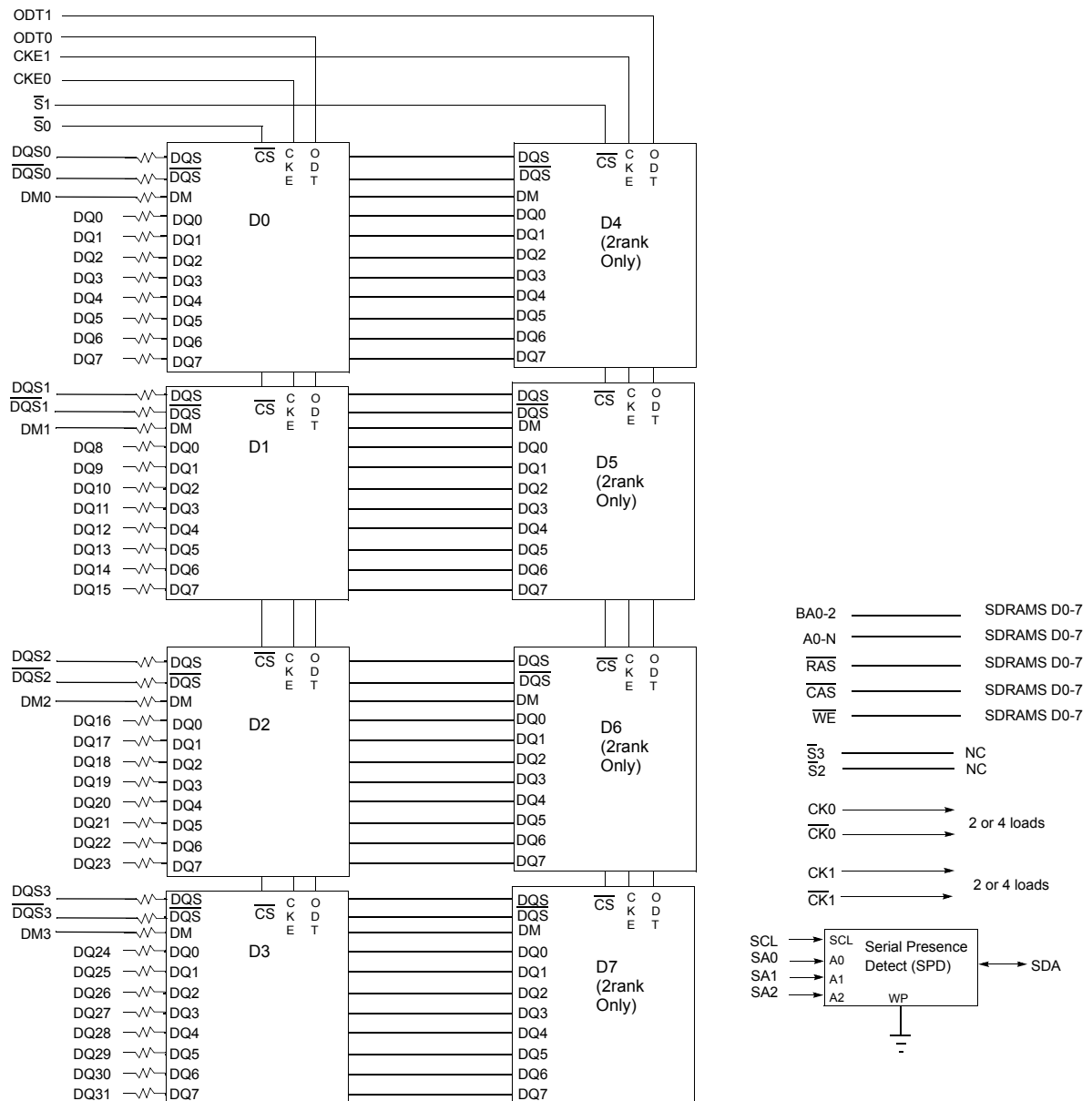
Note: For future compatibility, systems should ground undriven address and bank address inputs.

Note:

Note:

Block Diagram: Raw Card Version A (Populated as 1 or 2 rank of x16 SDRAMs)

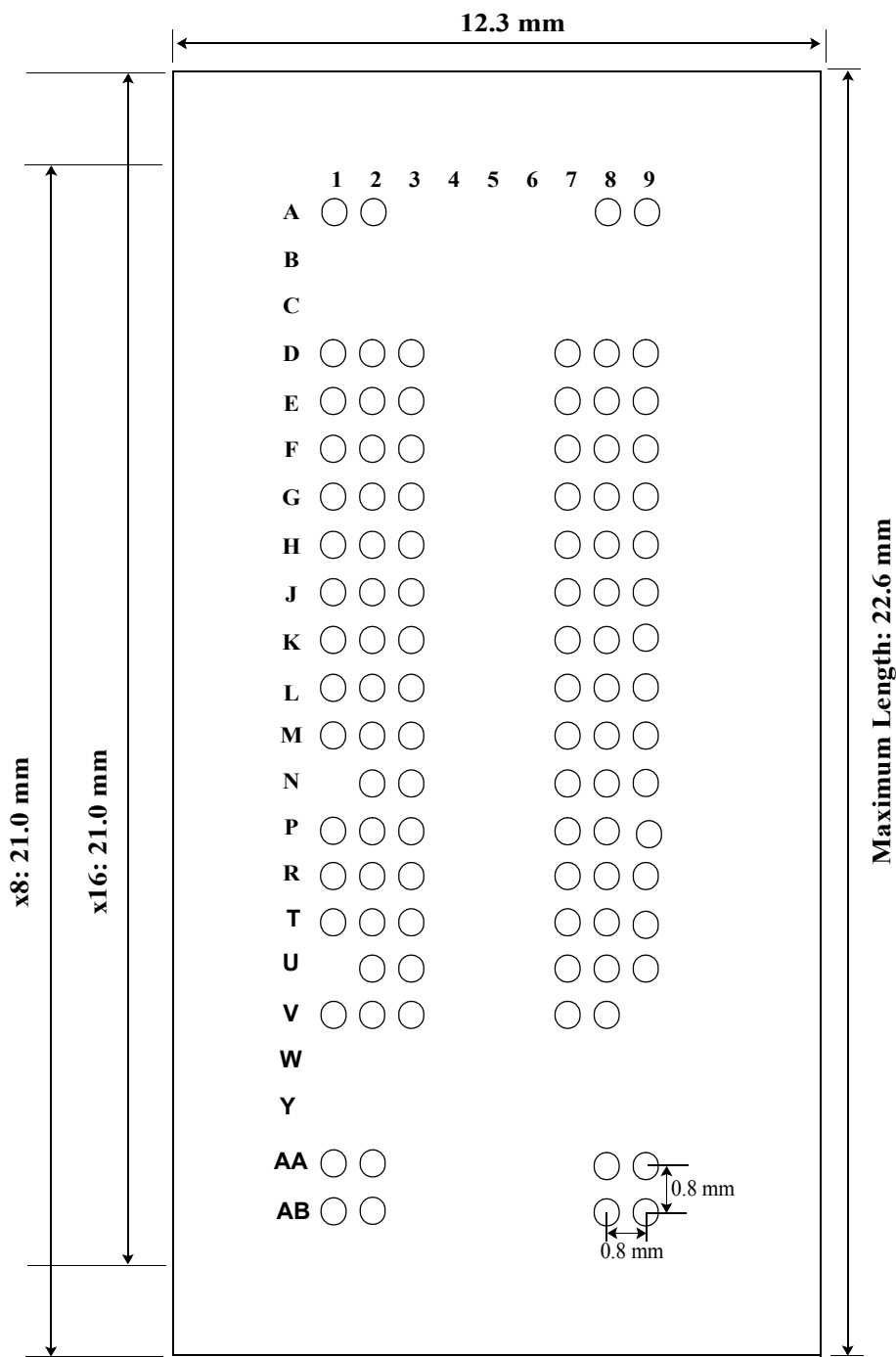
Block Diagram: Raw Card Version B (Populated as 1 or 2 rank of x8 SDRAMs)



#Unless otherwise noted, resistor values are 22 $\Omega \pm 5\%$
DQ wiring may differ from that described in this drawing; however, DQ/DM/DQS relationships are maintained as shown

4. Component Details

32b-SO-DIMM Common ball pattern for x8 and x16 - 256Mb, 512Mb, 1Gb DDR SDRAM Planar Components (Top View)



x8 Ballout for 256Mb, 512Mb, 1Gb, 2Gb and 4Gb DDR2 SDRAMs (Top View)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
VDD	NC	VSS	D	VSSQ	NC	VDDQ
NC	NC	NC	E	NC	NC	NC
NC	NC	NC	F	NC	NC	NC
NC	NC	NC	G	NC	NC	NC
VDD	NU/RDQS	VSS	H	VSSQ	DQS	VDDQ
DQ6	VSSQ	DM/RDQS	J	DQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	K	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	L	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	M	VSSDL	CK	VDD
	CKE0	WE	N	RAS	CK	ODT
BA2	BA0	BA1	P	CAS	CS0	CS1
CKE1	A10	A1	R	A2	A0	VDD
VSS	A3	A5	T	A6	A4	ODT1
	A7	A9	U	A11	A8	VSS
VDD	A12	A14	V	A15	A13	
			W			
			Y			
NC	NC		AA		NC	NC
NC	NC		AB		NC	NC

x16 Ballout for 256Mb, 512Mb, 1Gb, 2Gb and 4Gb DDR2 SDRAMs (Top View)

1	2	3		7	8	9
NC	NC		A		NC	NC
			B			
			C			
VDD	NC	VSS	D	VSSQ	$\overline{\text{UDQS}}$	VDDQ
UDQ6	VSSQ	UDM	E	UDQS	VSSQ	UDQ7
VDDQ	UDQ1	VDDQ	F	VDDQ	UDQ0	VDDQ
UDQ4	VSSQ	UDQ3	G	UDQ2	VSSQ	UDQ5
VDD	NC	VSS	H	VSSQ	$\overline{\text{LDQS}}$	VDDQ
LDQ6	VSSQ	LDM	J	LDQS	VSSQ	LDQ7
VDDQ	LDQ1	VDDQ	K	VDDQ	LDQ0	VDDQ
LDQ4	VSSQ	LDQ3	L	LDQ2	VSSQ	LDQ5
VDDL	VREF	VSS	M	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	N	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	P	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10	A1	R	A2	A0	VDD
VSS	A3	A5	T	A6	A4	
	A7	A9	U	A11	A8	VSS
VDD	A12	A14	V	A15	A13	
			W			
			Y			
NC	NC		AA		NC	NC
NC	NC		AB		NC	NC

DDR2 SDRAM FBGA Component Specifications

The DDR2 SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC MO-207, variations DL-Z, DK-Z, DM-Z, DJ-Z. The MO-207 specification allows for a maximum component width of 12.5 mm. The DDR2 32b-SO-DIMM is designed for a maximum component width of 12.3mm and a maximum length of 21.0mm. Components used on DDR2 32b-SO-DIMMs are also limited to a maximum height (as shown in dimension "A" of MO-207) of 1.2 mm.

Reference SPD Component Specifications

The Serial Presence Detect EEPROMs have their own power pin, V_{DDSPD} , so that they can be programmed or read without powering up the rest of the module. The wide voltage range permits use with 1.8 V, 2.5 V or 3.3 V serial buses.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
V_{DDSPD}	Core Supply Voltage	1.7	3.6	V

5. Unbuffered 32b-SO-DIMM Details

DDR SDRAM Module Configurations (Reference Designs)

Raw Card	32b-SO-DIMM Capacity	32b-SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of banks in SDRAM	# Address bits row/col
A	64 MB	16 M x 32	256 Mbit	16 M x 16	2	1	BGA	4	13/9
A	128 MB	32 M x 32	256 Mbit	16 M x 16	4	2	BGA	4	13/9
A	128 MB	32 M x 32	512 Mbit	32 M x 16	2	1	BGA	4	13/10
A	256 MB	64 M x 32	512 Mbit	32 M x 16	4	2	BGA	4	13/10
A	256 MB	64 M x 32	1 Gbit	64 M x 16	2	1	BGA	8	13/10
A	512 MB	128 M x 32	1 Gbit	64 M x 16	4	2	BGA	8	13/10

Raw Card	32b-SO-DIMM Capacity	32b-SO-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of banks in SDRAM	# Address bits row/col
B	128 MB	16 M x 32	256 Mbit	32 M x 8	4	1	BGA	4	13/10
B	256 MB	32 M x 32	256 Mbit	32 M x 8	8	2	BGA	4	13/10
B	256 MB	32 M x 32	512 Mbit	64 M x 8	4	1	BGA	4	14/10
B	512 MB	64 M x 32	512 Mbit	64 M x 8	8	2	BGA	4	14/10
B	512 MB	64 M x 32	1 Gbit	128 M x 8	4	1	BGA	8	14/10
B	1024 MB	128 M x 32	1 Gbit	128 M x 8	8	2	BGA	8	14/10

Input Loading Matrix

Signal Names	Input Device	R/C A	R/C B
Clock (CK0, CK0)	SDRAM	1 or 2	2 or 4
Clock (CK1, CK1)	SDRAM	1 or 2	2 or 4
S0/S1	SDRAM	0 or 2	0 or 4
S2/S3	SDRAM	0	0
CKE0/CKE1/ODT0/ODT1	SDRAM	0 or 2	0 or 4
Addr/RAS/CAS/BA/WE	SDRAM	2 or 4	4 or 8
DQ/DQS/DQS/DM	SDRAM	1 or 2	1 or 2
SCL/SDA/SA	SPD	1	1

DDR 32b-SO-DIMM Gerber File Releases

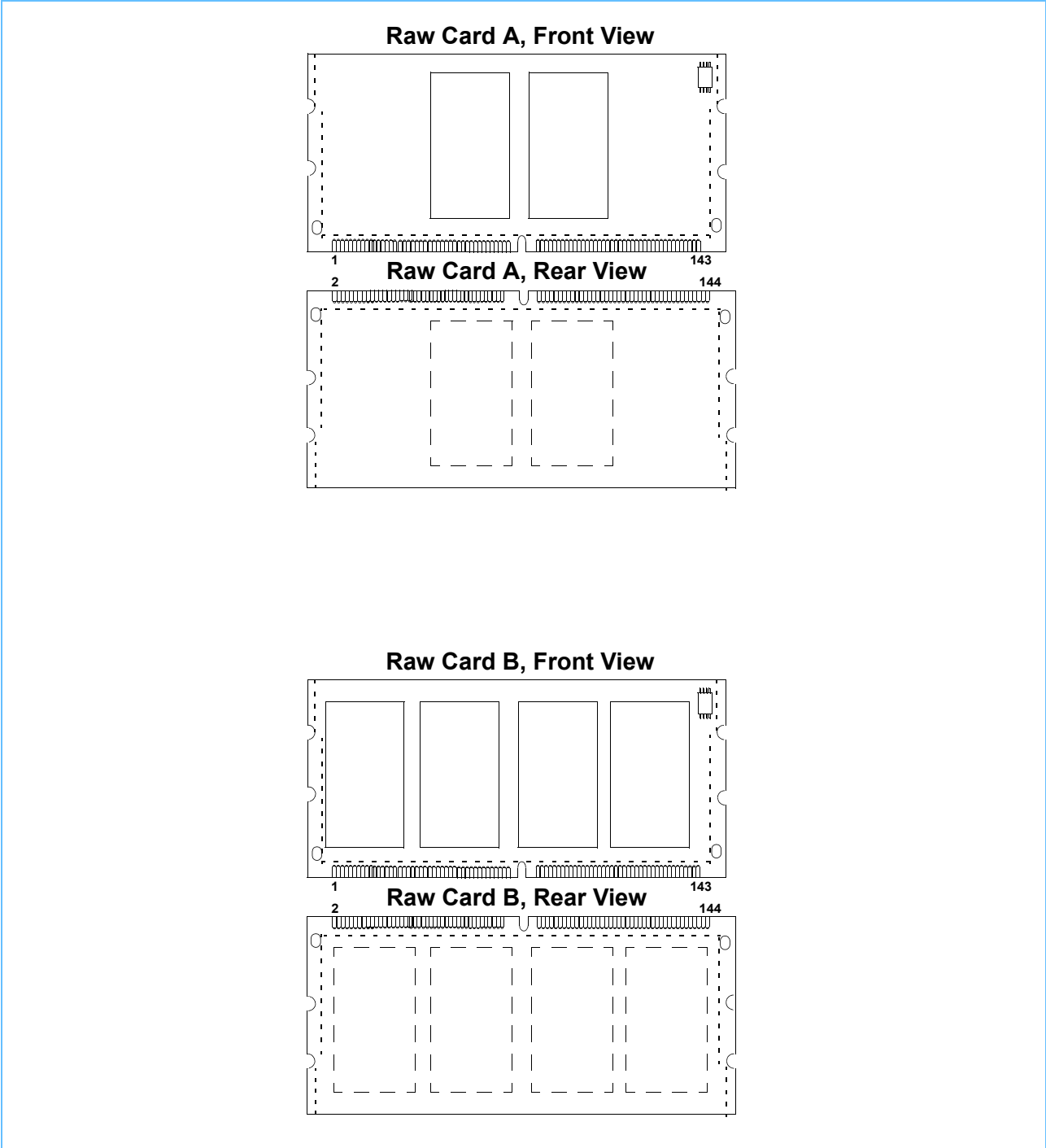
Reference design file updates will be released as needed. This specification will reflect the most recent design files, but may be updated to reflect clarifications to the specification only; in these cases, the design files will not be updated. The following table outlines the most recent design file releases

Note: Future design file releases will include both a date and a revision label. All changes to the design file are also documented within the 'read-me' file.

Raw Card	Specification Revision	Applicable Design File	Note
A	0.31	0.3	
B	0.31	0.3	

Example Raw Card Component Placement

The component layout for Raw Card variants are similar whether SDRAMs are populated on front side only or on front and back sides. Passive components are mounted on both sides of the board. This example is for reference only; refer to JEDEC standard MO-274 variation AA for details.



6. 32b-SO-DIMM Wiring Details

Signal Groups

This specification categorizes SDRAM timing-critical signals into four groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Page
Clock	CK [1:0], \overline{CK} [1:0]	17, 18
Data, Data Mask, Data Strobe	DQ [31:0], DM[3:0], DQS[3:0], \overline{DQS} [3:0]	19
Select, Clock Enable, Termination	\overline{S} [1:0], CKE [1:0], ODT[1:0]	20, 21
Address/Command	An, BAn, \overline{RAS} , \overline{CAS} , \overline{WE}	22, 23

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing recommendations are as follows. Other stackups and layouts are possible that meet the electrical characteristics.

- Route all signal traces except clocks using 4 mil rules, 4 mil minimum spacing between adjacent traces.
- Route clocks as much as possible using the inner layers.
- Test points are required on all signal groups.

Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered 32b-SO-DIMM designs. The diagrams should be used to determine individual signal wiring on a 32b-SO-DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify 32b-SO-DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one DDR2s SDRAM input unless specified as two loads (stacked DRAM has two loads). It is highly recommended that the net structure routing data in this document be simulated by the user.

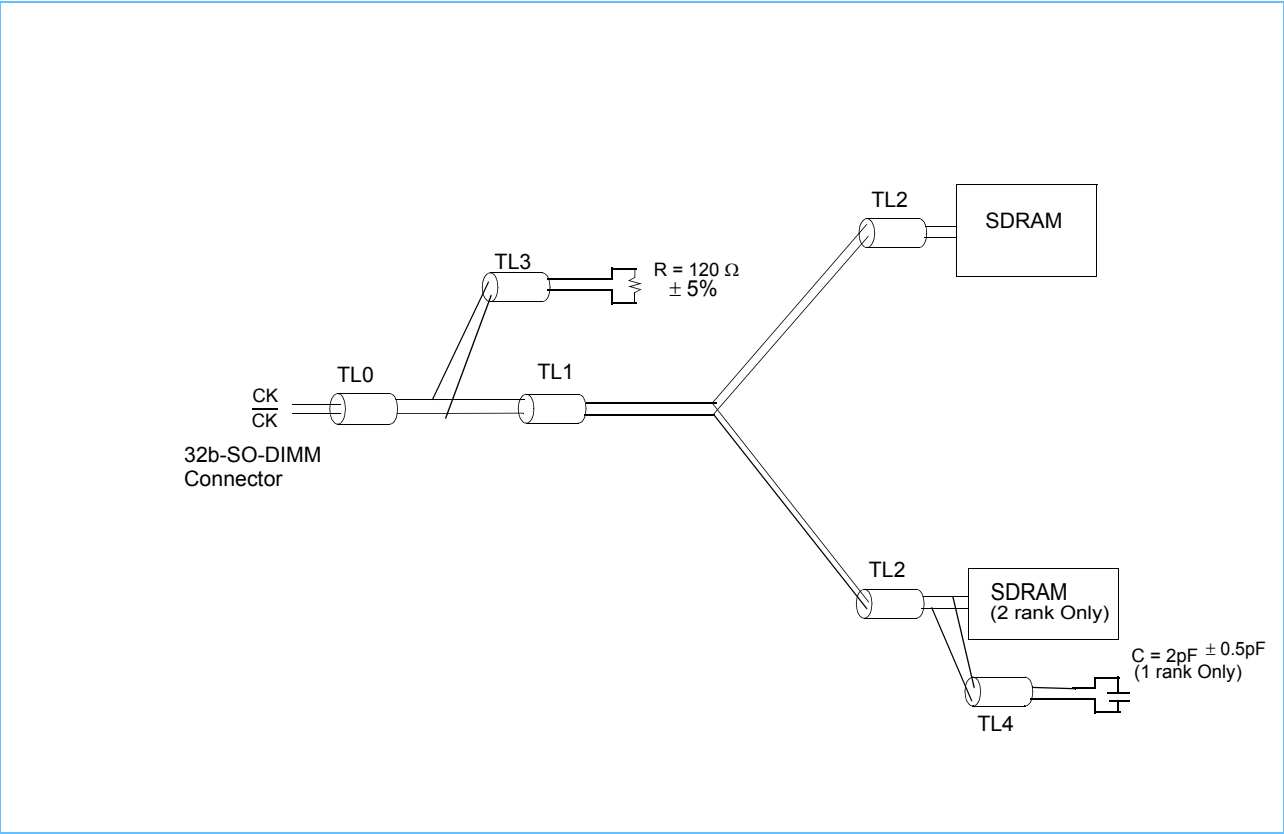
Differential Clock Net Structures

CK[1:0], $\overline{\text{CK}}[1:0]$

DDR SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair in the SDRAM
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54 mm total) between clocks of the same function

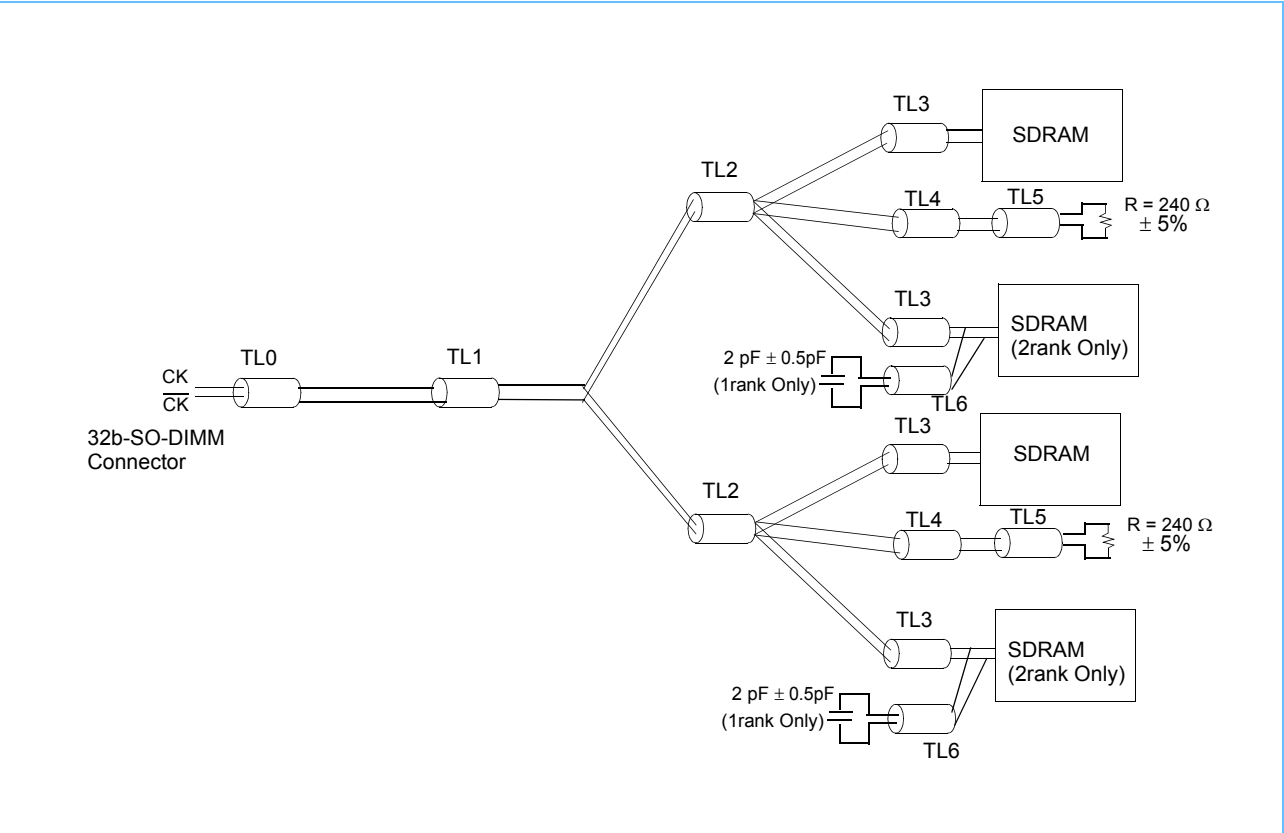
Clock Net Wiring CK[1:0], $\overline{\text{CK}}[1:0]$ (Raw Card A)



Clock Routing Trace Lengths

Raw card	TL0 Outer		TL1 Inner		TL2 Outer		TL3 Outer		TL4 Outer		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A	3.9	4.1	54.9	55.1	3.5	3.7	0.5	1.0	0.5	1.0	1
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeters.											

Clock Net Wiring CK[1:0], $\overline{\text{CK}}[1:0]$ (Raw Card B)



Clock Routing Trace Lengths

Raw card	TL0 Outer		TL1 Inner		TL2 Inner		TL3 Outer		TL4 inner		TL5 Outer		TL6 Outer		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
B	1.9	2.1	14.8	15.1	8.2	8.5	3.8	4.0	7.1	7.3	0.5	1.0	0.5	1.0	1

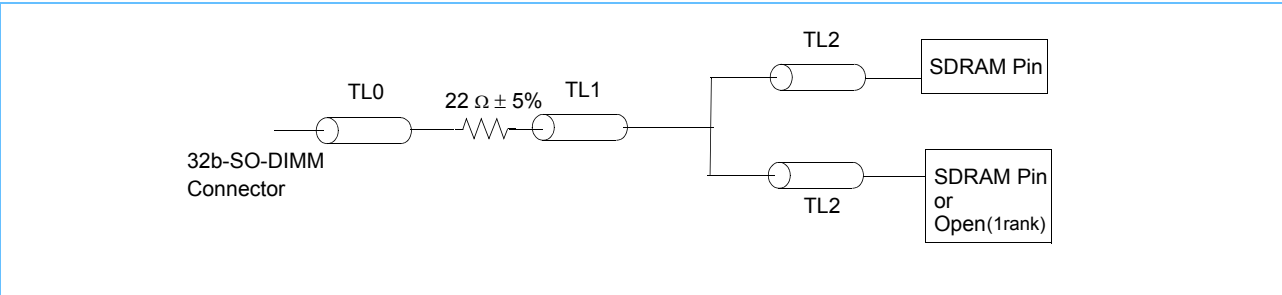
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeters

Data Net Structures

DQ[31:0], DM[3:0], DQS[3:0], $\overline{\text{DQS}}[3:0]$

Special attention has been paid to balancing the data nets within a DDR2 SDRAM, within a particular 32b-SO-DIMM, and across the 32b-SO-DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. It is recommend to maintain consistent delays for all nets as described in the following tables.

Net Structure Routing for DQ[31:0], DM[3:0], DQS[3:0], $\overline{\text{DQS}}[3:0]$ (Raw cards A, B)



Trace Lengths for Data Net Structure

Raw card	TL0 Outer		TL1 Outer		TL2 Outer		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A	3.0	5.0	20.0	23.0	0.5	3.0	26.3	26.5	1,2,3,4
B	3.0	4.0	14.0	17.0	0.5	3.0	20.5	20.7	1,2,3,4

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeters

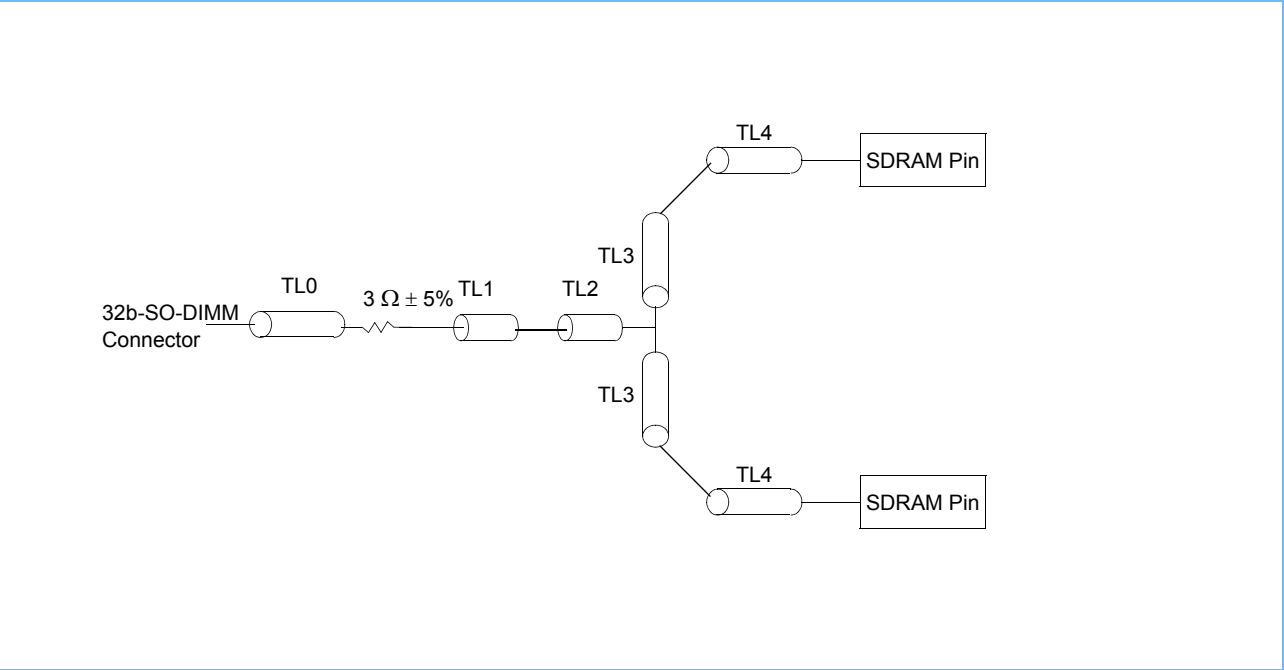
2. Total Min and Total Max refer to the min and max respectively of TL0 + TL1 + TL2

3. Given for lines without any via. For each via the line length must be reduced by 1.905 mm.

4. These signals must be referenced to ground

Control Net Structures \overline{S} [1:0], CKE[1:0], ODT[1:0] (Raw card A)

Net Structure Routing for Control nets

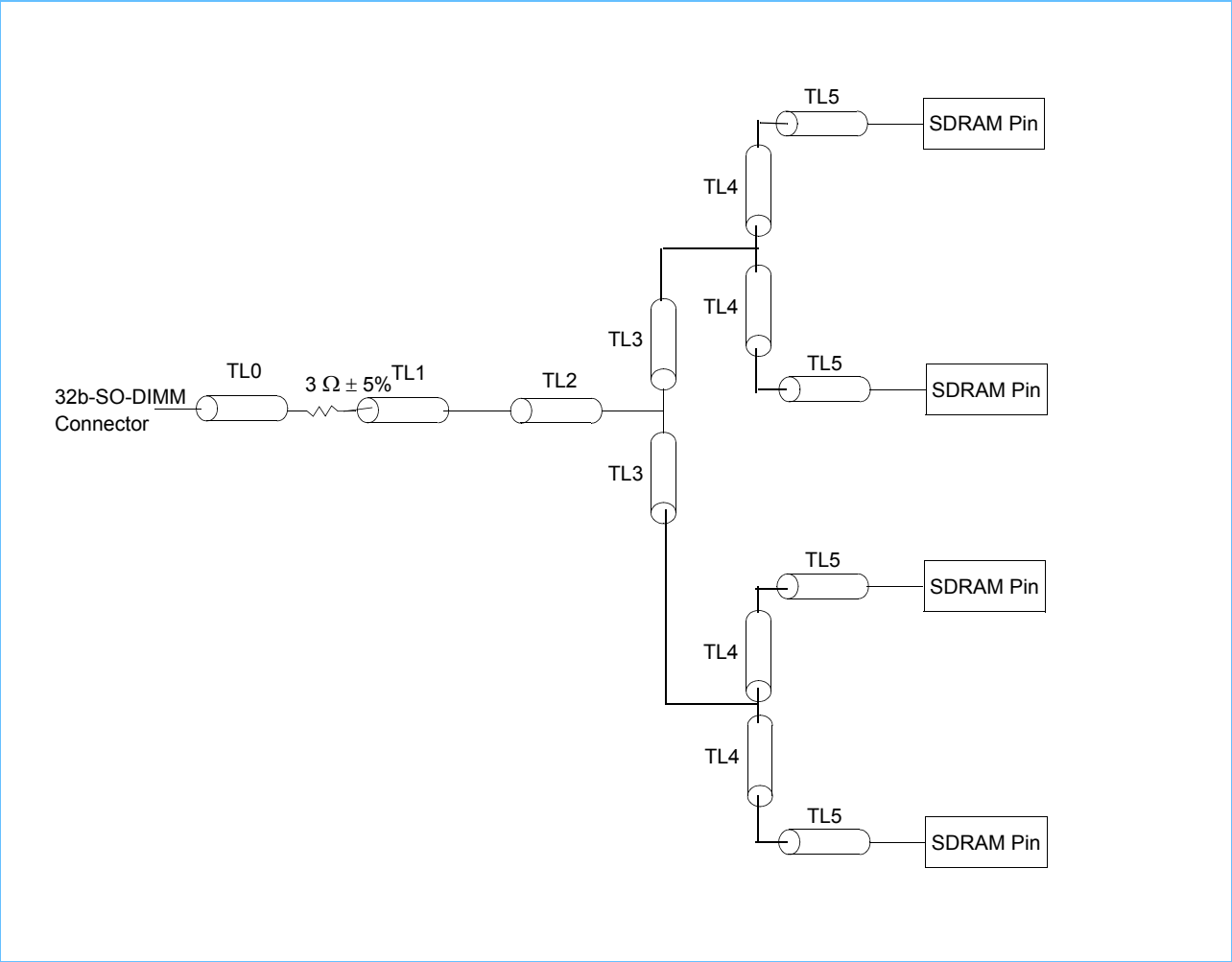


Trace Lengths for Control Net Structures

	TL0 Outer		TL1 Outer		TL2 Inner		TL0+TL1+TL2		TL3 Inner		TL4 Outer		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
A	3.0	5.5	0.7	10.5	75.0	90.0	90.0	95.0	14.8	15.8	0.5	3.0	1
1. All distances are given in mm and should be kept within a tolerance of ± 0.8 mm.													

Control Net Structures \overline{S} [1:0], CKE[1:0], ODT[1:0] (Raw card B)

Net Structure Routing for Control Nets

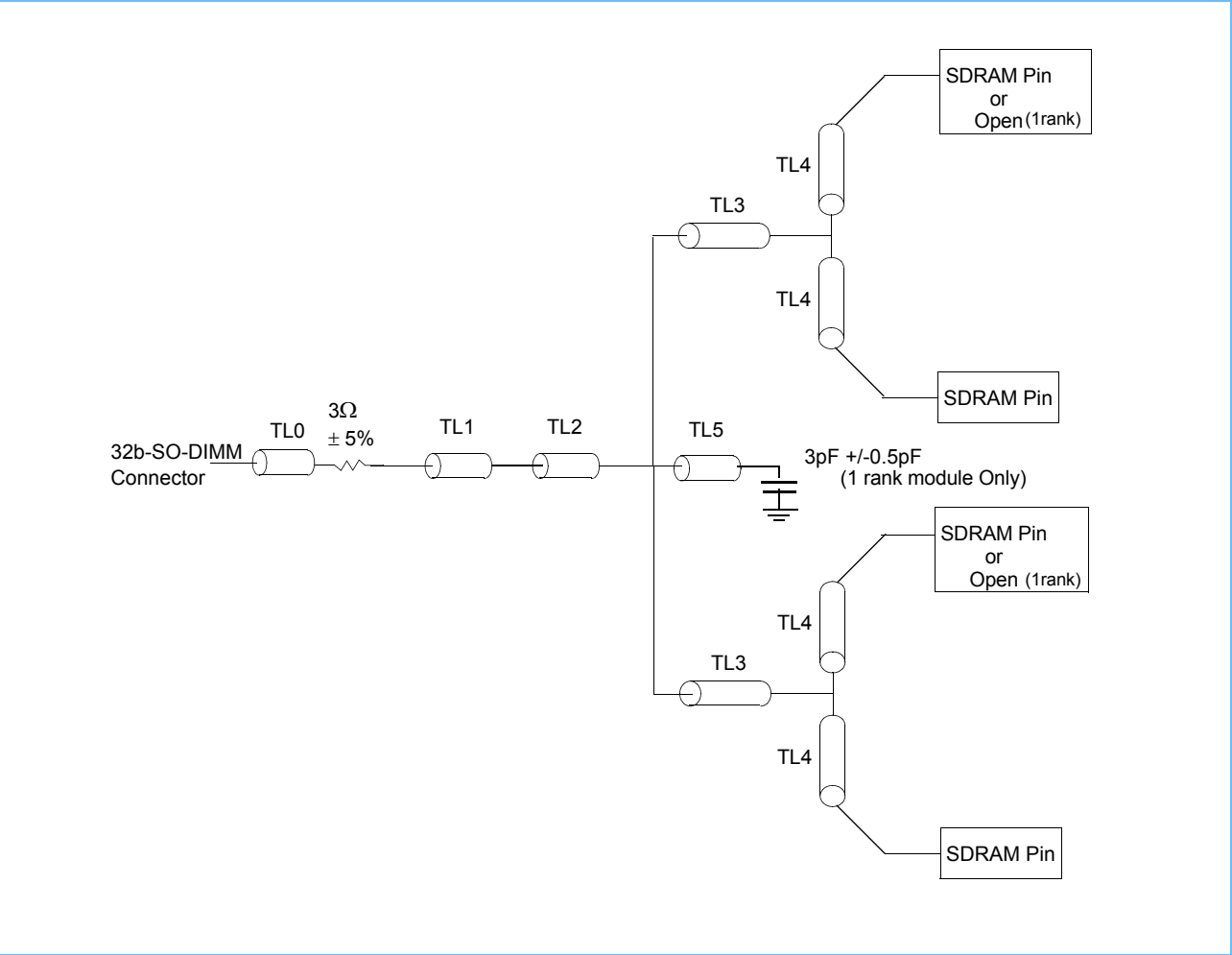


Trace Lengths for Control Net Structure

	TL0 Outer		TL1 Outer		TL2 Inner		TL0+TL1+TL2		TL3 Inner		TL4 Inner		TL5 Outer	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
B	3.0	5.0	0.8	40	0	37.1	41.0	43.5	17.2	20.2	7.0	10.0	0.5	4.0
1. All distances are given in mm and should be kept within a tolerance of ± 0.8 mm														

Address/Command Net Structures Ax, BAx, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ (Raw card A)

Net Structure Routing for Address and Command

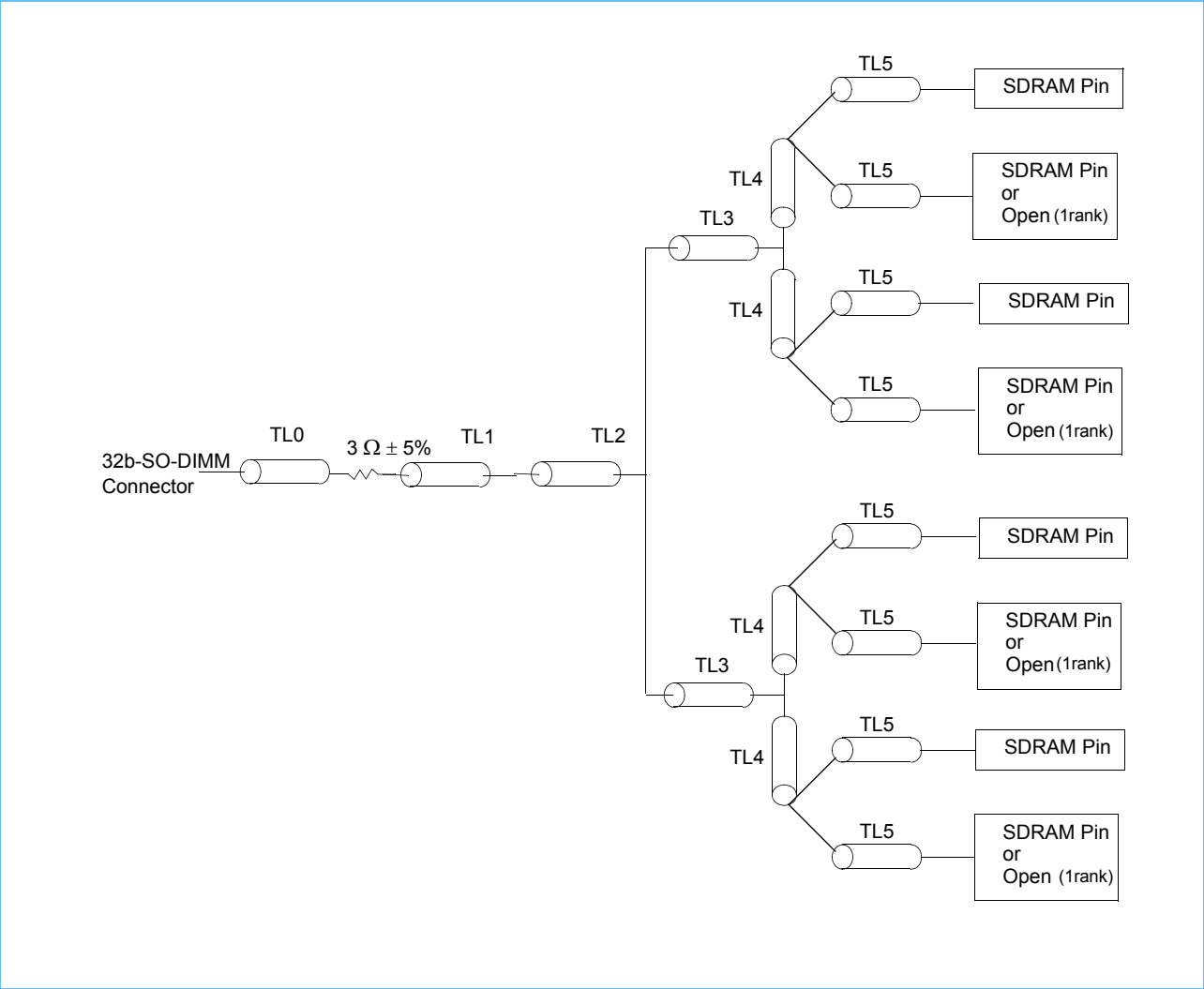


Trace Lengths for Address and Command Net Structures

Raw Card	TL0 Outer		TL1 Outer		TL2 Inner		TL0+TL1+TL2		TL3 Inneer		TL4 Outer		TL5 Outer	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	3.0	4.6	0.8	91.0	0	87.0	90.0	95.0	14.8	16.2	1.0	7.0	0.9	5.0
1. All distances are given in mm and should be kept within a tolerance of ± 0.8 mm														

Address/Command Net Structures Ax, BAx, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ (Raw card B)

Net Structure Routing for Address and Command



Trace Lengths for Address and Command Net Structures

	TL0 Outer		TL1 Outer		TL2 Inner		TL0+TL1+TL2		TL3 Inner		TL4 Inner		TL5 Outer	
Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
B	3.0	4.5	0.5	40.0	0	37.0	41.0	43.2	17.8	20.2	7.0	9.5	0.9	6.0
1. All distances are given in mm and should be kept within a tolerance of ± 0.8 mm														

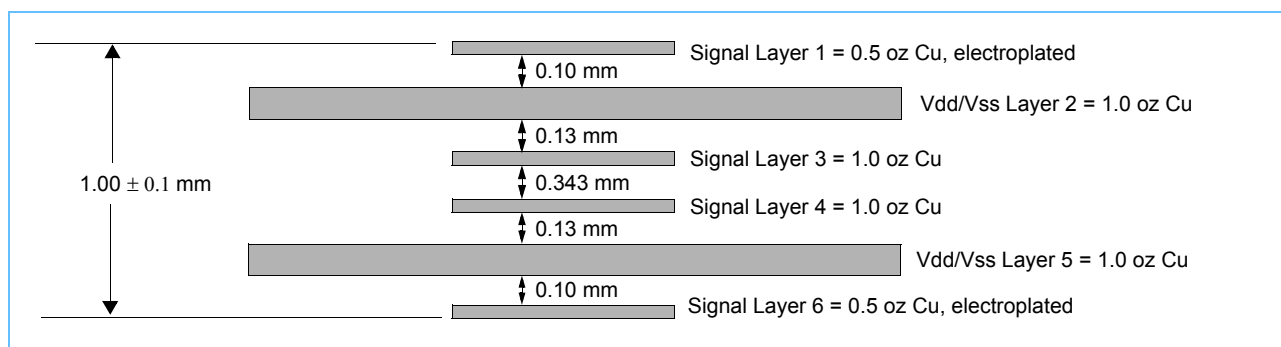
Cross Section Recommendations

The DDR2 32b-SO-DIMM printed circuit board design uses six-layers of glass epoxy material. Layers 2 and 4 are divided so adjacent signal layers maintain a constant Vss or Vdd reference. All data is referenced to Vss and all address/command are referenced to Vdd. The PCB stackup must be designed with 4 mil wide traces. The required board impedance is $60 \Omega \pm 10\%$.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	5.5	6.7	ps/mm
Trace velocity: S0 (inner layers)	6.5	7.6	ps/mm
Trace impedance: Z0 (all layers)	54	66	Ohms

Example Layer Stackup



Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices, especially for VREF, must be practically located near the device power pins.

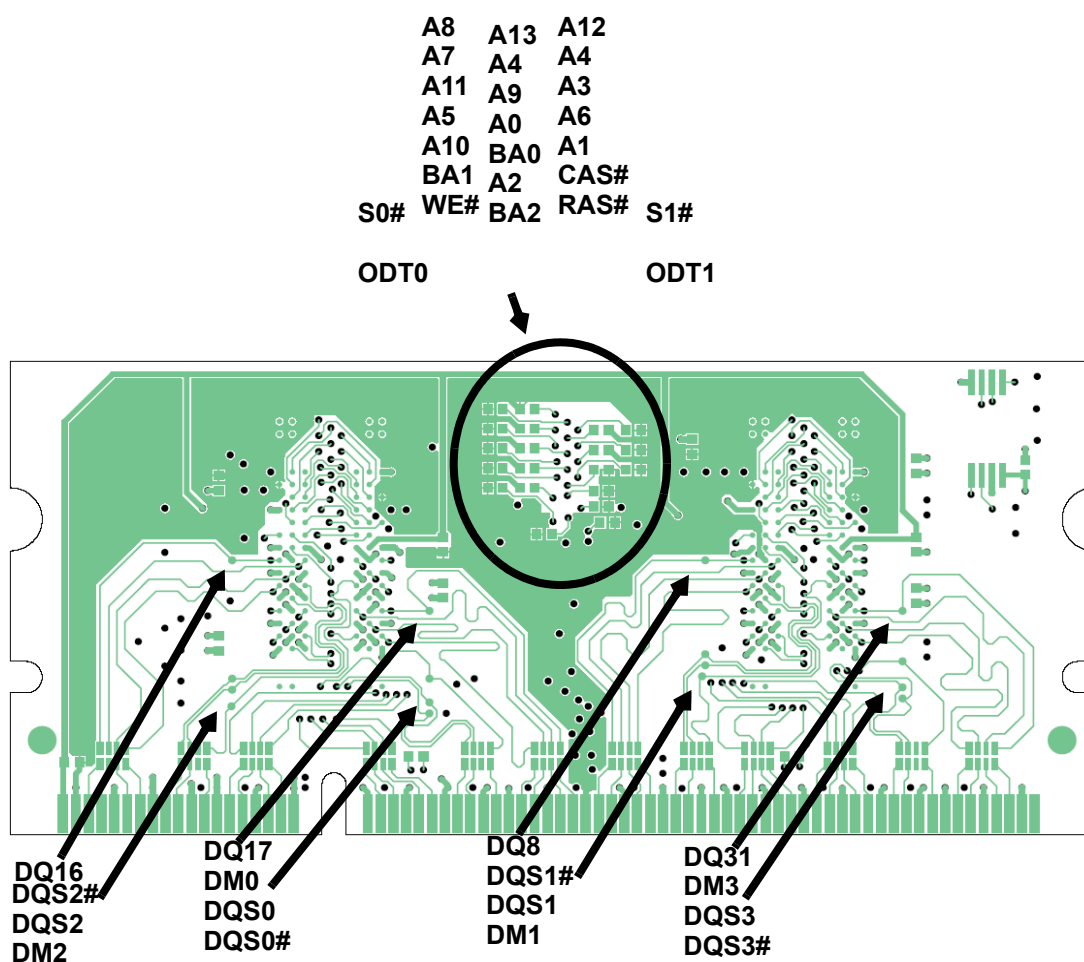
7. Test Points

All DDR2 components are in BGA packages which makes the package pads inaccessible for probing during system development. The DDR2 32b-SO-DIMMs have test points identified to make initial evaluation easier. In some cases test pads have been added and in other cases existing vias are used as test points. An effort has been made to provide testability on some signals in all signal groups but 100% coverage is not possible.

Raw Card A Test Points

The test point coverage for RC A is on the front side of the card. The following figures detail the locations of the test points.

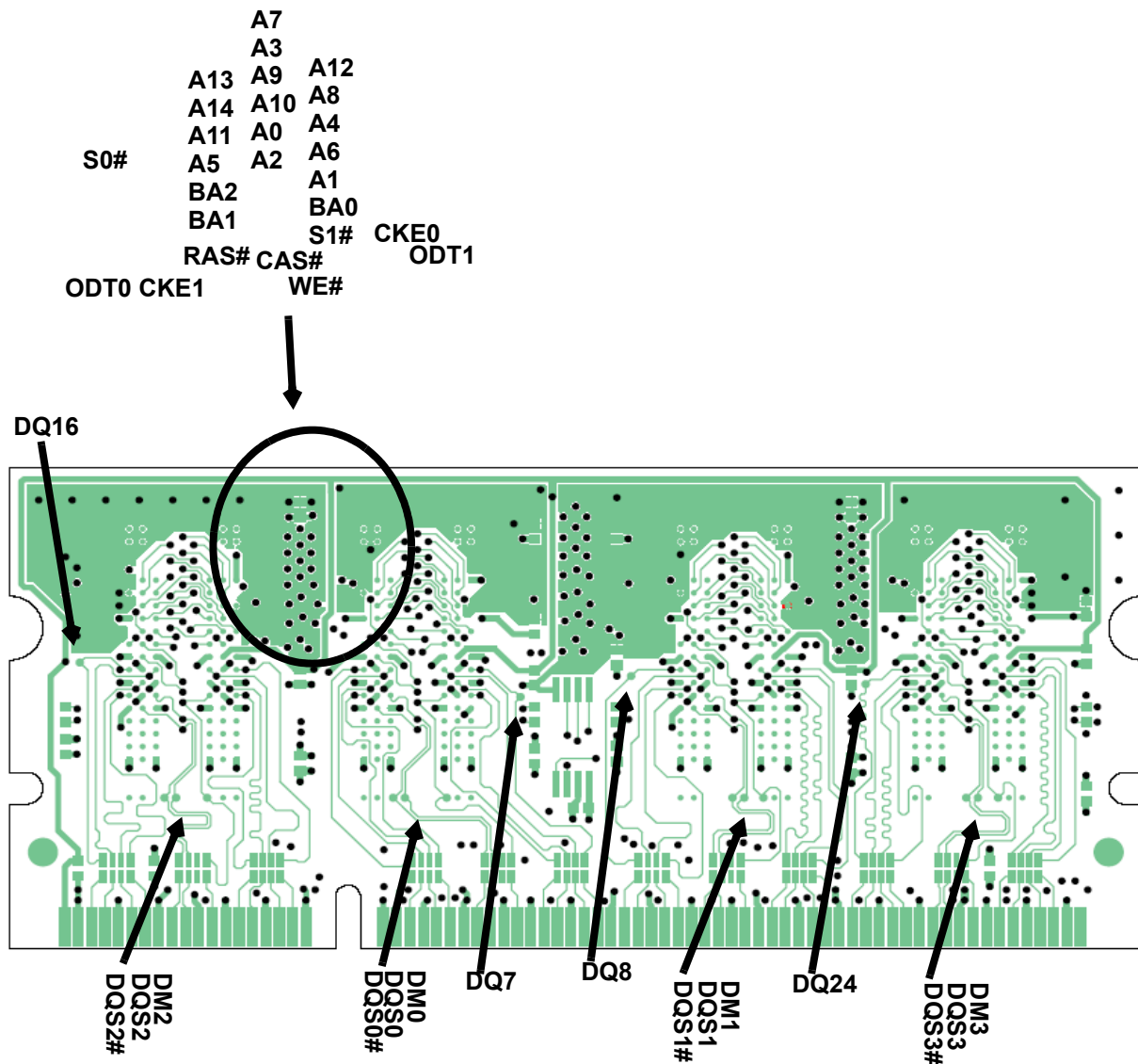
Raw Card A Front View



Raw Card B Test Points

The test point coverage for RC B is on the front side of the card. The following figures detail the locations of the test points.

Raw Card B Front View



If the SDRAMs are longer than 16.0mm (this is rare), some test points will be under SDRAM. In this case, use Rpack as the test points.

8. Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the EP2-2100 DDR2 SDRAM 32b-SO-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR2 SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of a typical EP2-2100 DDR2 32b-SO-DIMM. SPD values indicating different 32b-SO-DIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or 32b-SO-DIMMs. This example assumes:

- Module Organization: 256 MB
- Device Composition: 32Mx16
- Device Package: BGA
- Module Physical Ranks: 2
- CAS latency: 3(DDR2-400)

Serial Presence Detect Data Example (Part 1 of 3)

Byte # (dec)	Byte # (hex)	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
			DDR2-400	DDR2-400	
0	00	Number of Serial PD Bytes written during production	128	80	1
1	01	Total Number of Bytes in Serial PD device	256	08	2
2	02	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2, ...)	DDR2 SDRAM	08	
3	03	Number of Row Addresses on Assembly	13	0D	
4	04	Number of Column Addresses on Assembly	10	0A	
5	05	Number of DIMM Ranks	Module height: 30 mm, Planar, card on card: no, 2Rank	61	
6	06	Data Width of this Assembly	x32	20	
7	07	Reserved	Undefined	00	
8	08	Voltage Interface Level of this assembly	SSTL 1.8V	05	
9	09	SDRAM Cycle Time at maximum supported $\overline{\text{CAS}}$ latency (CL), CL = X	5.0 ns	50	3
10	0A	SDRAM Access from Clock	+/-0.45 ns	45	
11	0B	DIMM configuration type (Non-parity, or ECC)	Non-Parity	00	
12	0C	Refresh Rate/Type	7.8 us	82	3,4
13	0D	Primary SDRAM Width	x16	10	
14	0E	Error Checking SDRAM Width	NA	00	
15	0F	Reserved	Undefined	00	
16	10	SDRAM device attributes: Burst lengths supported	4,8	0C	

1. This will typically be programmed as 128 bytes.
2. This will typically be programmed as 256 bytes.
3. From Data sheet.
4. High order bit is self refresh "flag". If set to "1", the assembly supports self refresh.
5. These are optional, in accordance with the JEDEC specification.

Serial Presence Detect Data Example (Part 2 of 3)

Byte # (dec)	Byte # (hex)	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
			DDR2-400	DDR2-400	
17	11	SDRAM device attributes: Number of Banks on SDRAM device	4	04	3
18	12	SDRAM device attributes: $\overline{\text{CAS}}$ Latency	5,4,3	38	3
19	13	Reserved	Undefined	00	0
20	14	DIMM type information	SO-DIMM	04	
21	15	SDRAM Module Attributes	Normal DIMM	00	
22	16	SDRAM device attributes: General	Suports weak drivet	01	
23	17	Minimum Clock Cycle at CL=X -1	5.0 ns	3D	3
24	18	Maximum Data Access Time (t_{AC}) from Clock at CL=X -1	500 ps	50	3
25	19	Minimum Clock Cycle Time at CL=X-2	5 ns	50	3
26	1A	Maximum Data Access Time (t_{AC}) from Clock at CL=X-2	600 ps	60	3
27	1B	Minimum Row Precharge Time (t_{RP})	15.0 ns	3C	3
28	1C	Minimum Row Active to Row Active delay (t_{RRD})	7.5 ns	1E	3
29	1D	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD})	15.0 ns	2D	3
30	1E	Minimum Active to Precharge Time (t_{RAS})	45.0 ns	2D	3
31	1F	Module Rank Density	128 MB	20	
32	20	Address and Command input Setup Time Before Clock (t_{IS})	250 ps	25	3
33	21	Address and Command input Hold Time After Clock (t_{IH})	500 ps	27	3
34	22	Data Input Setup Time Before Strobe (t_{DS})	300 ps	05	3
35	23	Data Input Hold Time After Strobe (t_{DH})	300 ps	17	3
36	24	Write recovery time (t_{WR})	15.0 ns	3C	3
37	25	Internal write to read command delay (t_{WTR})	7.5 ns	1E	3
38	26	Internal read to precharge command delay (t_{RTP})	7.5 ns	1E	3
39	27	Memory analysis probe characteristics	Undefined	00	
40	28	Extension of byte 41 and 42.	41, 42 extension	00	
41	29	SDRAM device minimum active to active/auto refresh time (t_{RC})	60 ns	3C	3
42	2A	SDRAM device minimum auto-refresh to active/auto refresh command period (t_{RFC})	75 ns	4B	3
43	2B	SDRAM device maximum device cycle time (t_{CKmax})	8.0 ns	80	3

1. This will typically be programmed as 128 bytes.
2. This will typically be programmed as 256 bytes.
3. From Data sheet.
4. High order bit is self refresh "flag". If set to "1", the assembly supports self refresh.
5. These are optional, in accordance with the JEDEC specification.

Serial Presence Detect Data Example (Part 3 of 3)

Byte # (dec)	Byte # (hex)	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
			DDR2-400	DDR2-400	
44	2C	SDRAM device maximum skew between DQS and DQ signals	300 ps	19	3
45	2D	SDRAM device maximum read data hold skew factor (t_{QHS})	400 ps	23	3
46	2E	PLL relock time	Undefined	00	3
47 - XX	2F-XX	Reserved for IDD in SPD	Undefined	00	
XX - 61	XX-3D	Reserved	Undefined	00	
62	3E	SPD revision	1.1	1.1	
63	3F	Checksum for bytes 0-62	Checksum Data	Checksum	
64-71	40-47	Manufacturers' JEDEC ID Code			
72	48	Module Manufacturing Location			
73-90	49-5A	Module Part Number			5
91-92	5B-5C	Module Revision Code			5
93-94	5D-5E	Module Manufacturing Date	Year/Week code	yyww	5
95-98	5F-62	Module Serial Number	Serial Number	ssssssss	
99-127	63-7F	Manufacturer's Specific Data	Undefined	XX	5
128-255	80-FF	Open for Customer Use	Undefined	XX	
<ol style="list-style-type: none"> 1. This will typically be programmed as 128 bytes. 2. This will typically be programmed as 256 bytes. 3. From Data sheet. 4. High order bit is self refresh "flag". If set to "1", the assembly supports self refresh. 5. These are optional, in accordance with the JEDEC specification. 					

9. Product Label

The following label shall be applied to all DDR2 memory modules targeted at embedded market products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

ggggg eRxff EP2-wwwm-abc-ddeef

Where:

ggggg = Module total capacity, in bytes

256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed

1R = 1 rank of DDR2 SDRAM installed

2R = 2 ranks

4R = 4 ranks

xff = Device organization (bit width) of DDR2 SDRAMs used on this assembly

x4 = x4 organization (4 DQ lines per SDRAM)

x8 = x8 organization

x16 = x16 organization

www = Module bandwidth in MB/s

1600 = 1.600 GB/s

2100 = 2.133 GB/s

m = Module Type

B = Unbuffered 32-bit Small Outline DIMM ("32b-SO-DIMM")

a = DDR2 SDRAM CAS Latency, in clocks at maximum operating frequency

b = DDR2 SDRAM minimum tRCD specification, in clocks at maximum operating frequency

c = DDR2 SDRAM minimum tRP specification, in clocks at maximum operating frequency

dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM

ee = Reference design file used for this design (if applicable)

-A = Reference design for raw card 'A' is used for this assembly

-B = Reference design for raw card 'B' is used for this assembly

AV = Reference design for raw card 'AV' is used for this assembly

-Z = None of the reference designs were used for this assembly

f = Revision number of the reference design used

0 = Initial release

1 = First revision

2 = Second revision

P = Pre-release or Engineering sample

Z = To be used when field e = Z

Examples, single font:**128MB 2Rx8 EP2-2100B-333-12-BP**

is a 128 MB DDR2 Unbuffered 32b-SO-DIMM using 2 ranks of x8 SDRAMs operational to EP2-2100 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.2, raw card reference design file B pre-release engineering sample layout used for the assembly

Examples, with font change:**64MB 1Rx16 EP2-2100B-333 12-A1**

is a 64 MB DDR2 32b-SO-CDIMM using 1 rank of x16 SDRAMs operational to EP2-2100 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.2, raw card reference design file A revision 1 used for the assembly

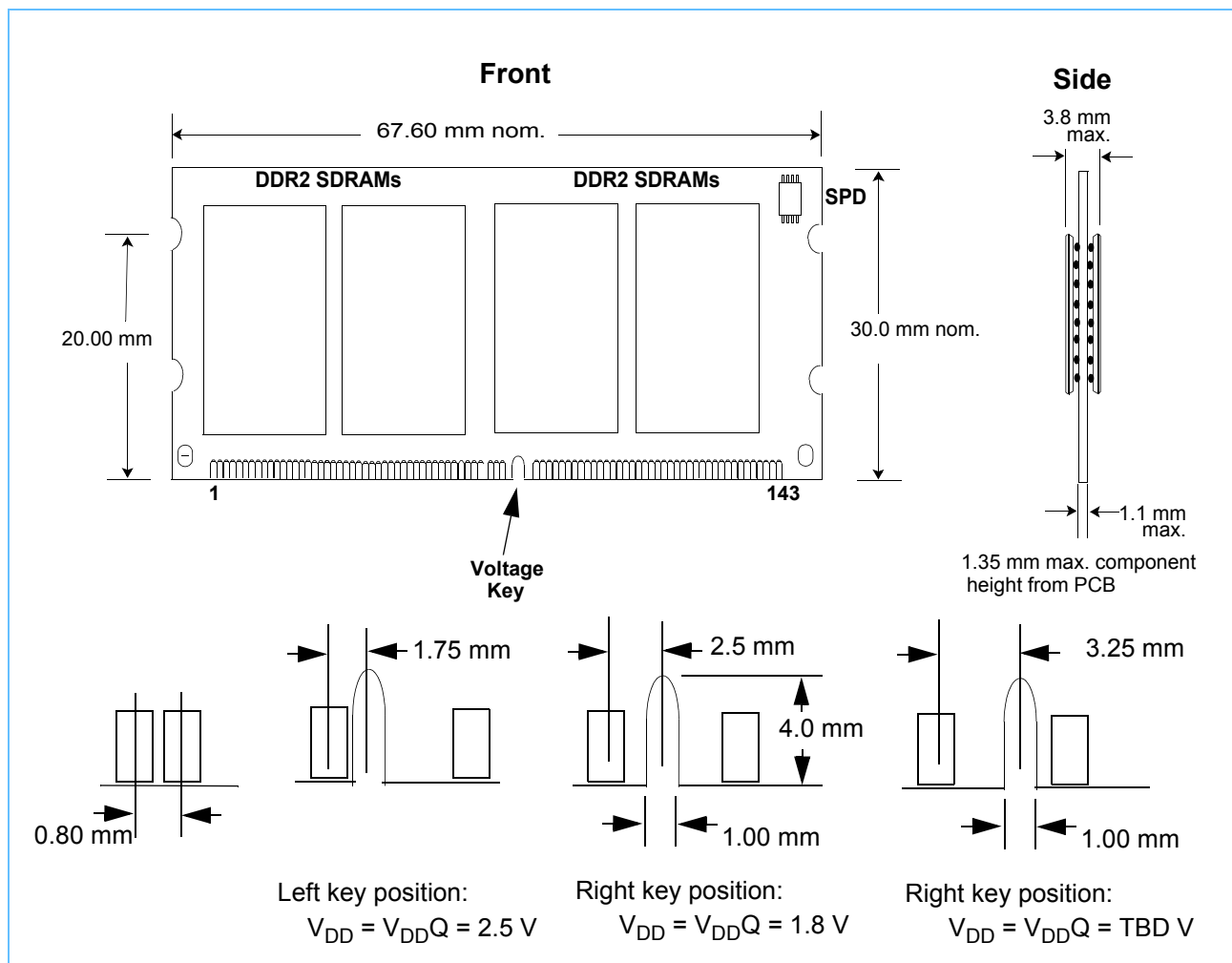
10. 32b-SO-DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 16b/32b 144 Pin SO-DIMM family. This information can be accessed on the worldwide web as follows: (This procedure is as of June/2006.)

1. Go to <http://www.jedec.org>.
2. Click on 'Free Standards' --> 'JEP95 MAIN PAGE' --> 'Microelec. Outlines'
3. Scroll down and select 'MO-274' to download the PDF for this product family.
4. Or you can search this document from 'Free Standards' top page.

This example is for reference only; please refer to JEDEC standard MO-274 variation AA for details.

Reference Simplified Mechanical Drawing with Keying Position



Revision History:

Date	Rev.	Page	Changes
1/March/2006	0.1	All	Initial draft
9/June/2006	0.3	All	fully revised.
20/June/2006	0.31	4	MO-number corrected
		14	input loading matrix corrected
		16	Signal Group reference page number filled
		17-23	Updated trace lengths and topology drawings
28/June/2006	0.9	30	Corrected the definition of "ee"
		All	Minor clean ups
26/Sept./2006	1.0	4, 15, 32	Corrected "MO-273" to "MO-274"(Ballot comment)
		10	Corrected "Common landing pattern" to " Common ball pattern"(Ballot comment)
5/Oct/2006	1.0	4, 19, 27	Added space between digits and units.
		30	Deleted typographical error data in label.